ML12179
500-2800 MHz Single Channel Frequency Synthesizer

Legacy Device: *Motorola MC12179*

The ML12179 is a monolithic Bipolar synthesizer integrating the high frequency prescaler, phase/frequency detector, charge pump, and reference oscillator/buffer functions. When combined with an external loop filter and VCO, the ML12179 serves as a complete PLL subsystem. The device is designed for operation up to 2.8 GHz for high frequency applications such as CATV down converters and satellite receiver tuners.

- 2.8 GHz Maximum Operating Frequency
- Low Power Supply Current of 3.5 mA Typical, Including I_{CC} and Ip Current
- Supply Voltage of 5.0 V Typical
- Integrated Divide by 256 Prescaler
- On–Chip Reference Oscillator/Buffer
  - 2.0 to 11 MHz Operation When Driven From Reference Source
  - 5.0 to 11 MHz Operation when used with a Crystal
- Digital Phase/Frequency Detector with Linear Transfer Function
- Balanced Charge Pump Output
- Space Efficient 8–Lead SOIC
- Operating Temperature Range T_A = –40° to +85°C

SO 8 = -5P
PLASTIC PACKAGE
CASE 751
(SO–8)

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
SO 8	MC12179D	ML12179-5P

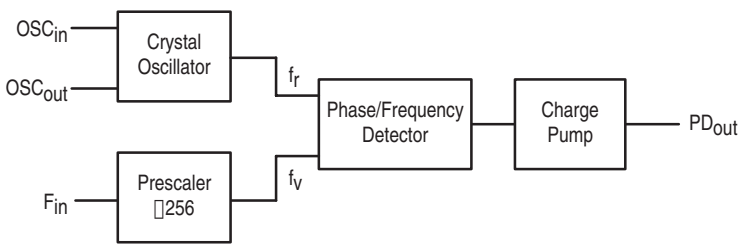
Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

MAXIMUM RATINGS (Note 1)

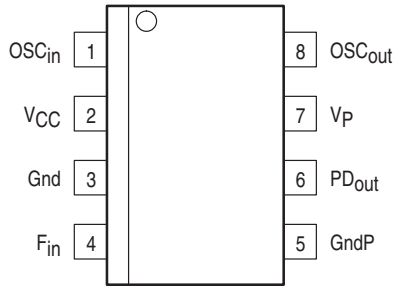
Parameter	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	–0.5 to 6.0	Vdc
Power Supply Voltage, Pin 7	V_P	V_{CC} to 6.0	Vdc
Storage Temperature Range	Tstg	–65 to 150	□C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions as identified in the Electrical Characteristics table.

Block Diagram



PIN CONNECTIONS



(Top View)

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; V_P = V_{CC} to 5.5 V; T_A = –40 to 85 C, unless otherwise noted.)

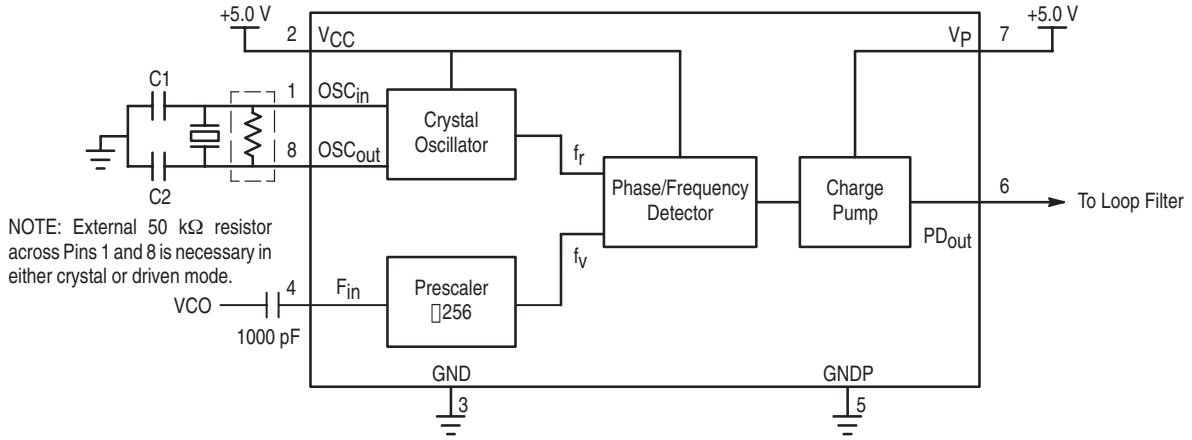
Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Supply Current for V_{CC}	I_{CC}	–	3.1	5.6	mA	Note 1
Supply Current for V_P	I_P	–	0.4	1.3	mA	Note 1
Operating Frequency $f_{IN}max$ $f_{IN}min$	F_{IN}	2800 –	– –	– 500	MHz	Note 2
Operating Frequency Crystal Mode External Oscillator OSC_{in}	F_{OSC}	5 2	– –	11 11	MHz	Note 3 Note 4
Input Sensitivity F_{in}	V_{IN}	200	–	1000	$mV_{P–P}$	Note 2
Input Sensitivity External Oscillator OSC_{in}	V_{OSC}	500	–	2200	$mV_{P–P}$	Note 4
Output Source Current[5] (PD_{out})	I_{OH}	–2.8	–2.2	–1.6	mA	V_P = 4.5 V, V_{PDout} = V_P/2
Output Sink Current[5] (PD_{out})	I_{OL}	1.6	2.2	2.8	mA	V_P = 4.5 V, V_{PDout} = V_P/2
Output Leakage Current (PD_{out})	I_{OZ}	–	0.5	15	nA	V_P = 5.0 V, V_{PDout} = V_P/2

NOTES: 1. V_{CC} and V_P = 5.5 V; F_{IN} = 2.56 GHz; F_{OSC} = 10 MHz crystal; PD_{out} open.
2. AC coupling, F_{IN} measured with a 1000 pF capacitor.
3. Assumes C_1 and C_2 (Figure 1) limited to 30 pF each including stray and parasitic capacitances.
4. AC coupling to OSC_{in}.
5. Refer to Figure 15 and Figure 16 for typical performance curves over temperature and power supply voltage.

PIN FUNCTION DESCRIPTION

Pin	Symbol	I/O	Function
1	OSCin	I	Oscillator Input – An external parallel–resonant, fundamental crystal is connected between OSC_{in} and OSC_{out} to form an internal reference oscillator (crystal mode). External capacitors C1 and C2, as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. For an external reference oscillator, an external signal is AC–coupled to the OSC_{in} pin with a 1000 pF coupling capacitor, with no connection to OSC_{out}. In either mode, a resistor with a nominal value of 50 kΩ MUST be placed across the OSC_{in} and OSC_{out} pins for proper operation.
2	V_{CC}	–	Positive Power Supply. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.
3	Gnd	–	Ground.
4	F_{in}	I	Prescaler Input – The VCO signal is AC coupled into the F_{in} pin.
5	GndP	–	Ground – For charge pump circuitry .
6	PD_{out}	O	Single ended phase/frequency detector output (charge pump output). Three–state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.
7	V_P	–	Positive power supply for charge pump. V_P MUST be equal or greater than V_{CC}. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.
8	OSCout	O	Oscillator output, for use with an external crystal as shown in Figure 1.

Figure 1. ML12179 Expanded Block Diagram



PHASE CHARACTERISTICS

The phase comparator in the ML12179 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. The detector can cover a range of ±2π radian of fv/fr phase difference. The operation of the charge pump output is shown in Figure 2.

fr lags fv in phase OR fv>fr in frequency

When the phase of fr lags that of fv or the frequency of fv is greater than fr, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

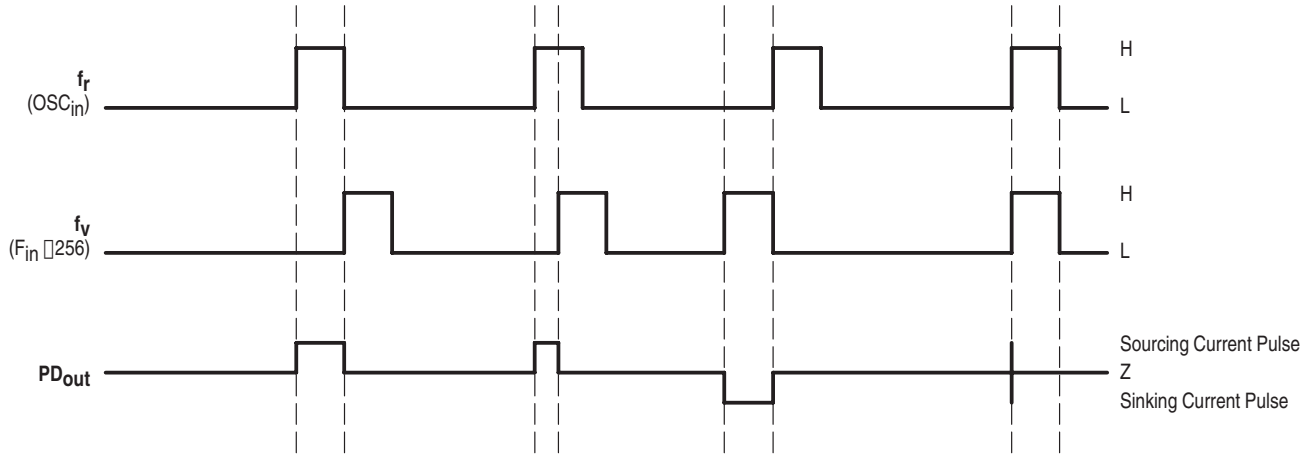
fr leads fv in phase OR fv<fr in frequency

When the phase of fr leads that of fv or the frequency of fv is less than fr, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

fr = fv in phase and frequency

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

Figure 2. Phase/Frequency Detector and Charge Pump Waveforms

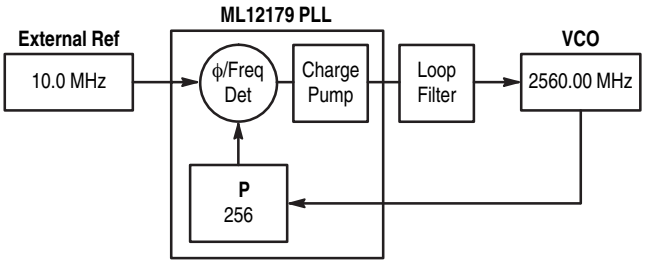


H = High voltage level; L = Low voltage level; Z = High impedance
NOTES: Phase difference detection range: ~ –2π to 2π

$$K_p\text{–Charge Pump Gain} \approx \frac{|I_{source}| + |I_{sink}|}{4\pi} = \frac{|2.2| + |-2.2|}{4\pi} = \frac{1.1\ mA}{\pi radian}$$

The ML12179 is intended for applications where a fixed local oscillator is required to be synthesized. The prescaler on the ML12179 operates up to 2.8GHz which makes the part ideal for many satellite receiver applications as well as applications in the 2nd ISM (Industrial, Scientific, and Medical) band which covers the frequency range of 2400MHz to 2483MHz. The part is also intended for MMDS (Multi–channel Multi–point Distribution System) block downconverter applications. Below is a typical block diagram of the complete PLL.

Figure 3. Typical Block Diagram of Complete PLL



As can be seen from the block diagram, with the addition of a VCO, a loop filter, and either an external oscillator or crystal, a complete PLL sub–system can be realized. Since most of the PLL function is integrated into the ML12179, the user's primary focus is on the loop filter design and the crystal reference circuit. Figure 13 and Figure 14 illustrate typical VCO spectrum and phase noise characteristics. Figure 17 and Figure 18 illustrate the typical input impedance versus frequency for the prescaler input.

Crystal Oscillator Design

The ML12179 is used as a multiply–by–256 PLL circuit which transfers the high stability characteristic of a low frequency reference source to the high frequency VCO in the PLL loop. To facilitate this, the device contains an input circuit which can be configured as a crystal oscillator or a buffer for accepting an external signal source.

In the external reference mode, the reference source is AC–coupled into the OSC_{in} input pin. The input level signal should be between 500–2200 mVpp. When configured with an external reference, the device can operate with input frequencies down to 2 MHz, thus allowing the circuit to control the VCO down to 512 MHz. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the input signal as it switches against the internal voltage reference.

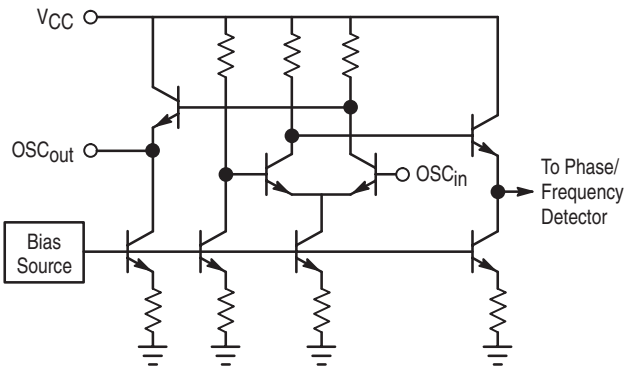
In the crystal mode, an external parallel–resonant fundamental mode crystal is connected between the OSC_{in} and OSC_{out} pins. This crystal must be between 5.0 MHz and 11 MHz. External capacitors, C1 and C2 as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen and the input capacitance of the device and any stray board capacitance.

In either mode, a 50kΩ resistor must be connected between the OSC_{in} and the OSC_{out} pins for proper device operation. The value of this resistor is not critical so a 47kΩ or 51kΩ ±10% resistor is acceptable.

Since the ML12179 is realized with an all–bipolar ECL style design, the internal oscillator circuitry is different from more traditional CMOS oscillator designs which realize the crystal oscillator with a modified inverter topology. These CMOS designs typically excite the crystal with a rail–to–rail signal which may overdrive the crystal resulting in damage or unstable operation. The ML12179 design does not exhibit these phenomena because the swing out of the OSC_{out} pin is less than 600mV. This has the added advantage of minimizing EMI and switching noise which can be generated by rail–to–rail CMOS outputs. The OSC_{out} output should not be used to drive other circuitry.

The oscillator buffer in the ML12179 is a single stage, high speed, differential input/output amplifier; it may be considered to be a form of the Pierce oscillator. A simplified circuit diagram is seen in Figure 4.

Figure 4. Simplified Crystal Oscillator/Buffer Circuit



OSC_{in} drives the base of one input of an NPN transistor differential pair. The non–inverting input of the differential pair is internally biased. OSC_{out} is the inverted input signal and is buffered by an emitter follower with a 70 □A pull–down current and has a voltage swing of about 600 mVpp. Open loop output impedance is about 425Ω. The opposite side of the differential amplifier output is used internally to drive another buffer stage which drives the phase/frequency detector. With the 50 kΩ feedback resistor in place, OSC_{in} and OSC_{out} are biased to approximately 1.1V below V_{CC}. The amplifier has a voltage gain of about 15 dB and a bandwidth in excess of 150 MHz. Adherence to good RF design and layout techniques, including power supply pin decoupling, is strongly recommended.

A typical crystal oscillator application is shown in Figure 1. The crystal and the feedback resistor are connected directly between OSC_{in} and OSC_{out}, while the loading capacitors, C1and C2, are connected between OSC_{in} and ground, and OSC_{out} and ground respectively. It is important to understand that as far as the crystal is concerned, the two loading capacitors are in series (albeit through ground). So when the crystal specification defines a specific loading capacitance, this refers to the total external (to the crystal) capacitance seen across its two pins.

This capacitance consists of the capacitance contributed by the amplifier (IC and packaging), layout capacitance, and the series combination of the two loading capacitors. This is illustrated in the equation below:

Legacy Applications Information

$$C_I = C_{AMP} + C_{STRAY} + \frac{C1 \times C2}{C1 + C2}$$

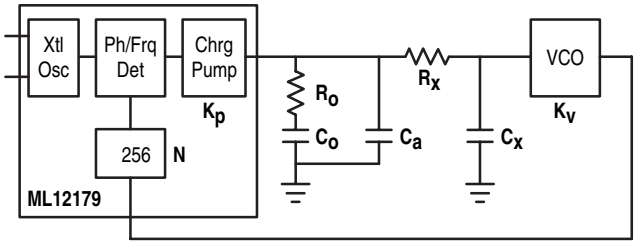
Provided the crystal and associated components are located immediately next to the IC, thus minimizing the stray capacitance, the combined value of C_{AMP} and C_{STRAY} is approximately 5pF. Note that the location of the OSC_{in} and OSC_{out} pins at the end of the package, facilitates placing the crystal, resistor and the C1 and C2 capacitors very close to the device. Usually, one of the capacitors is in parallel with an adjustable capacitor used to trim the frequency of oscillation. It is important that the total external (to the IC) capacitance seen by either OSC_{in} or OSC_{out}, be no greater than 30pF.

In operation, the crystal oscillator will start up with the application of power. If the crystal is in a can that is not grounded it is often possible to monitor the frequency of oscillation by connecting an oscilloscope probe to the can; this technique minimizes any disturbance to the circuit. If a malfunction is indicated, a high impedance, low capacitance, FET probe may be connected to either OSC_{in} or OSC_{out}. Signals typically seen at those points will be very nearly sinusoidal with amplitudes of roughly 300 to 600 mVpp. Some distortion is inevitable and has little bearing on the accuracy of the signal going to the phase detector.

Loop Filter Design

Because the device is designed for a non–frequency agile synthesizer (i.e., how fast it tunes is not critical) the loop filter design is very straight forward. The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated below in Figure 5.

Figure 5. Loop Filter



The R_O/C_O components realize the primary loop filter. C_a is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R_X/C_X realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a 4th order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a 2nd order loop (R_O/C_O) and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools can be used.

Component	Guideline
C_a	<0.1 x C_O
R_X	>10 x R_O
C_X	<0.1 x C_O

The focus of the design effort is to determine what the loop's natural frequency, ωo, should be. This is determined by R_O, C_O, K_p, K_V, and N. Because K_p, K_V, and N are given, it is only necessary to calculate values for R_O and C_O. There are 3 considerations in selecting the loop bandwidth:

1) Maximum loop bandwidth for minimum tuning speed
2) Optimum loop bandwidth for best phase noise performance
3)Minimum loop bandwidth for greatest reference sideband suppression

Usually a compromise is struck between these 3 cases, however, for the fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are 3 major sources of phase noise in the phase–locked loop – the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution equal to the total divide–by–N ratio. This is mathematically described in Figure 10. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. This is described in Figure 11. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15 dB has been selected, which corresponds to data in Figure 14.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturer. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the Crystal References increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 6.

The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. In the example of Figure 6, the optimum bandwidth is approximately 15 KHz.

Figure 6. Graphical Analysis of Optimum Bandwidth

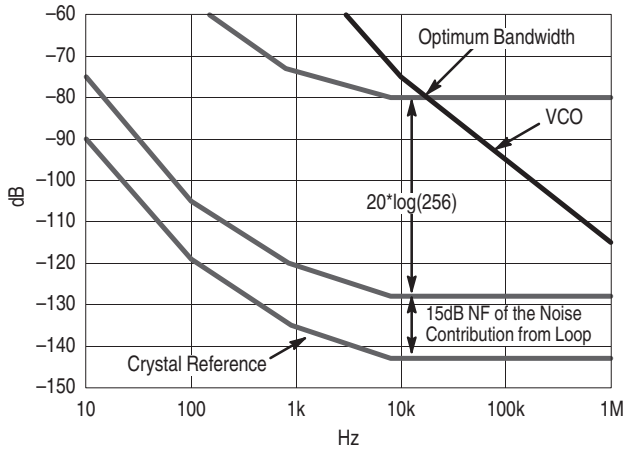
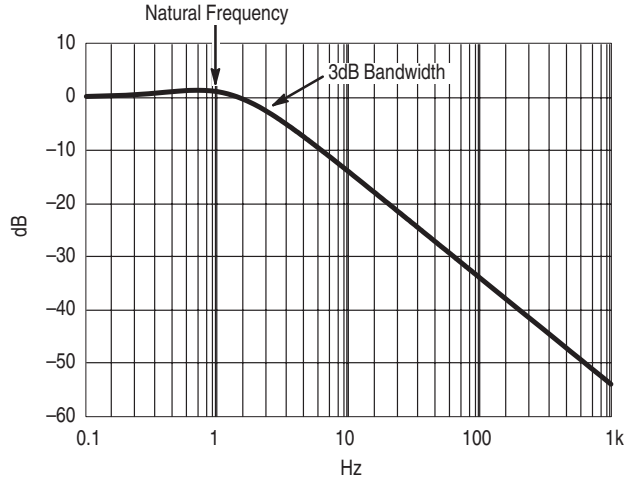


Figure 7. Closed Loop Frequency Response for ζ = 1



To simplify analysis further a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 7 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore the optimum loop bandwidth is15kHz/2.5 or 6kHz (37.7krads) with a damping coefficient, $\zeta \approx 1$. T(s) is the transfer function of the loop filter.

Figure 8. Design Equations for the 2nd Order System

$$T(s) = \frac{R_oC_os + 1}{\left(\frac{NC_o}{K_pK_v}\right)s^2 + R_oC_os + 1} = \frac{\left(\frac{2\zeta}{\omega_o}\right)s + 1}{\left(\frac{1}{\omega_o^2}\right)s^2 + \left(\frac{2\zeta}{\omega_o}\right)s + 1}$$

$$\left(\frac{NC_o}{K_pK_v}\right) = \left(\frac{1}{\omega_o^2}\right) \rightarrow \omega o = \sqrt{\frac{K_pK_v}{NC_o}} \rightarrow \boxed{C_o \quad \left(\frac{K_pK_v}{N\omega_o^2}\right)}$$

$$R_oC_o = \left(\frac{2\zeta}{\omega_o}\right) \rightarrow \zeta = \left(\frac{oR_oC_o}{2}\right) \rightarrow \boxed{R_o = \left(\frac{2\zeta}{\omega_oC_o}\right)}$$

In summary, follow the steps given below:

Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.

Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.

Step 3: Convert the divide–by–N to dB (20log 256 – 48 dB) and increase the phase noise of the crystal reference by that amount.

Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. This is approximately 15 kHz in Figure 6.

Step 5: Correlate this loop bandwidth to the loop natural frequency and select components per Figure 8. In this case the 3.0 dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3.0 dB loop bandwidth and the loop's "natural" frequency will vary for different values of ζ. Making use of the equations defined above in a math tool or spreadsheet is useful. To aid in the use of such a tool the equations are summarized in Figures 9 through 11.

Figure 9. Loop Parameter Relations

Let: $\frac{NC_o}{K_pK_v} = \frac{1}{\omega_o^2}$, $R_oC_o = \frac{2\zeta}{\omega_o}$

Let: $C_a = aC_o$, $C_x = bC_o$, $A = 1 + a$, and $B = 1 + a + b$

Let: $R_oC_o = \frac{1}{\omega_3}$, $R_xC_x = \frac{1}{\omega_4}$, $R_o(C_a + C_x) = \frac{1}{\omega_5}$

Let: $K_3\omega_3 = \omega_o$, $K_4\omega_4 = \omega_o$, $K_5\omega_5 = \omega_o$

Figure 10. Transfer Function for the Crystal Noise in the Frequency Plane

$$T(j\omega) = N \bullet \frac{1 + j\ (2\zeta\frac{\omega}{\omega_o})}{\left(1 + K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) + j\left(2\zeta\frac{\omega}{\omega_o} - (AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}$$

Figure 11. Transfer Function for the VCO Noise in the Frequency Plane

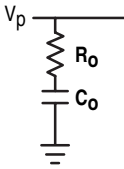
$$T(j\omega) = \frac{\left(K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) - j\left((AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}{\left(1 + K_3K_4\frac{\omega^4}{\omega_o{}^4} - B\frac{\omega^2}{\omega_o{}^2}\right) + j\left(2\zeta\frac{\omega}{\omega_o} - (AK_4 + K_5)\frac{\omega^3}{\omega_o{}^3}\right)}$$

Appendix: Derivation of Loop Filter Transfer Function

The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps. Step 1 is to find the voltage generated by the impedance of the loop filter. Step 2 is to find the transfer function from the input of the loop filter to its output. The "voltage" times the "transfer function" is the overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL multiply the filter's impedance by the gain constant of the phase detector then multiply that by the filter's transfer function (which is unity in the 2nd and 3rd order cases below).

Figure 12. Overall Transfer Function of the PLL

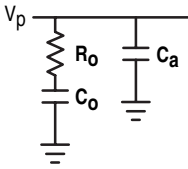
For the 2nd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_os}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

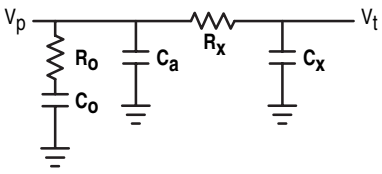
For the 3rd Order PLL:



$$Z_{LF}(s) = \frac{R_oC_os + 1}{C_oR_oC_as^2 + (C_o + C_a)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = 1\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

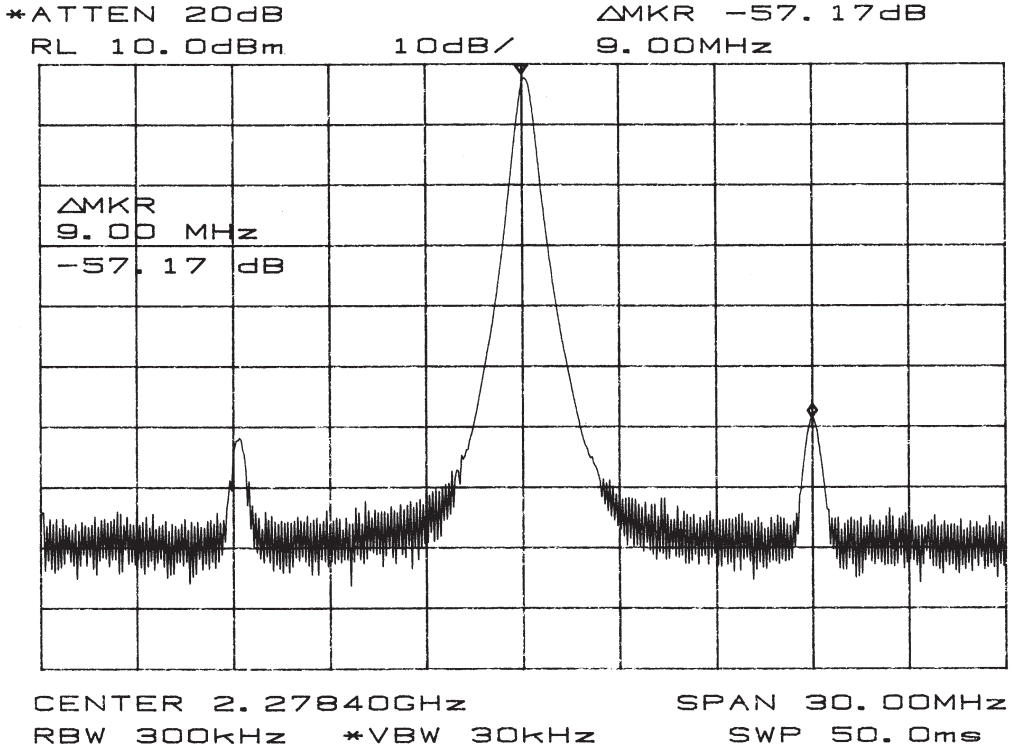
For the 4th Order PLL:



$$Z_{LF}(s) = \frac{(R_oC_os + 1)\ (R_xC_xs + 1)}{C_oR_oC_aR_xC_xs^3 + [\ (C_o + C_a)R_xC_x + C_oR_o(C_x + C_a)\ ]\ s^2 + (C_o + C_a + C_x)s}$$

$$T_{LF}(s) = \frac{V_t(s)}{V_p(s)} = \frac{1}{(R_xC_xs + 1)}\ ,\ V_p(s) = K_p(s)Z_{LF}(s)$$

Figure 13. VCO Output Spectrum with ML12179, V_{CC} = 5.0 V
(ECLiPTEK 8.9 MHz Crystal and ZCOM 2500 VCO)



NOTE: Spurs can be reduced further by narrowing the loop bandwidth of the PLL loop filter and/or adding an extra filter (R_X/C_X)

Figure 14. Typical Phase Noise Plot, 2200 MHz VCO
(With the ML12179 in a Closed Loop)

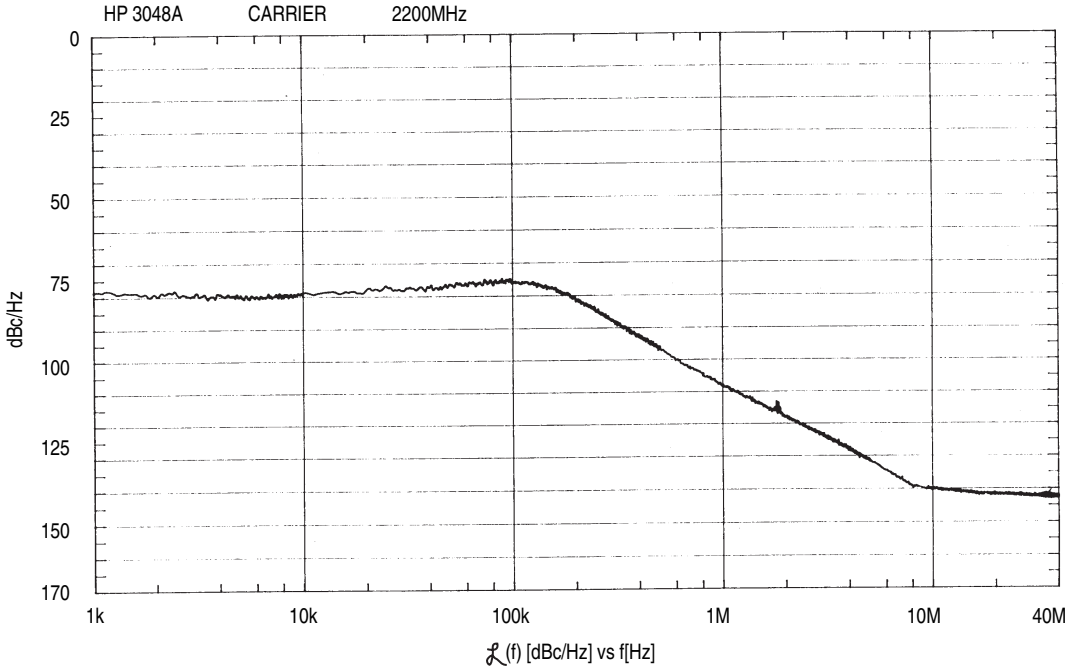


Figure 15. Typical Charge Pump Current versus Temperature
(V_{CC} = V_{pp} = 5.0 V)

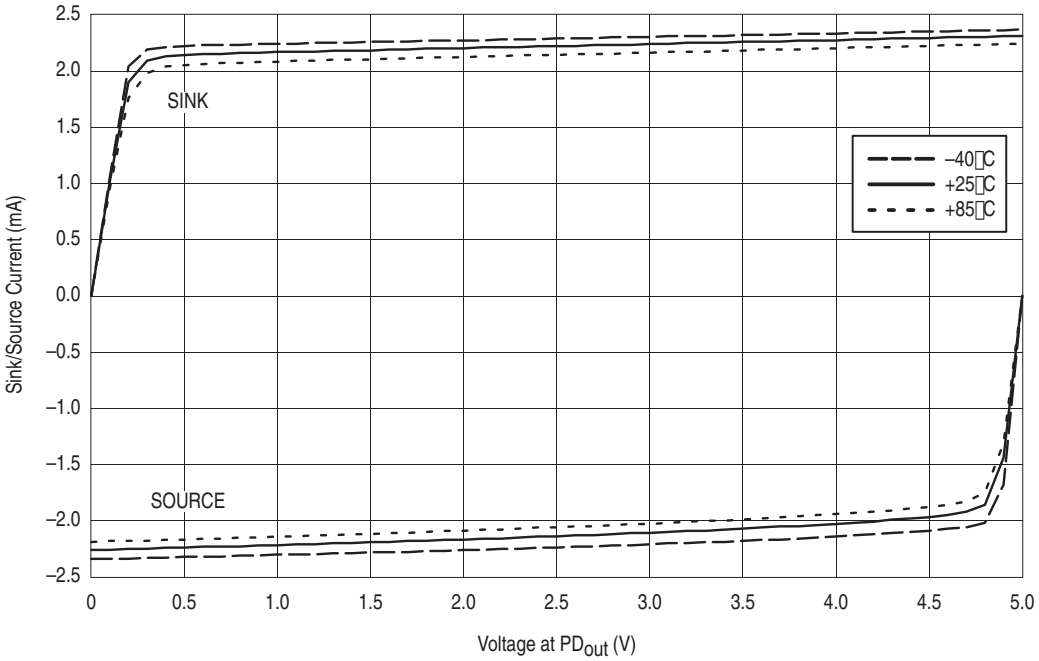


Figure 16. Typical Charge Pump Current versus Voltage
(T = 25°C)

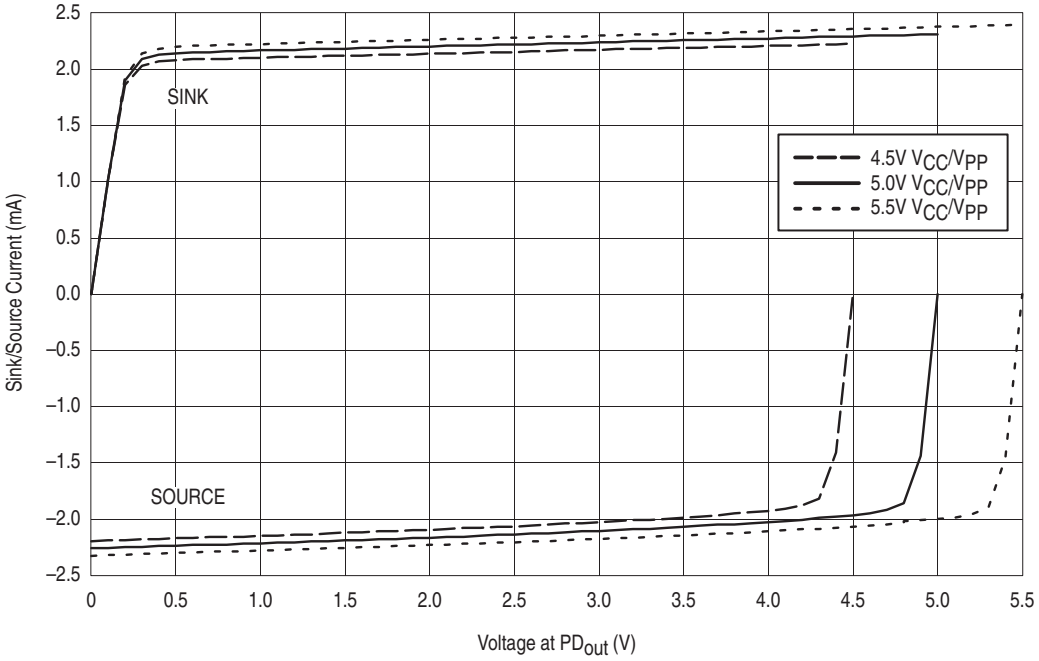


Figure 17. Typical Real Input Impedance versus Input Frequency
(For the F_{in} Input)

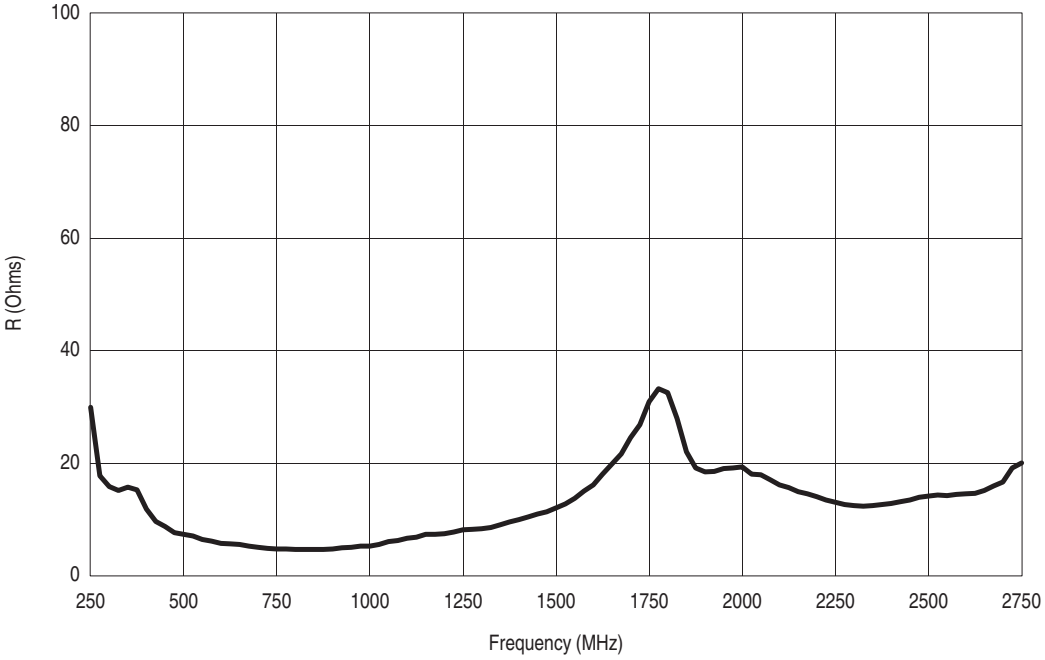
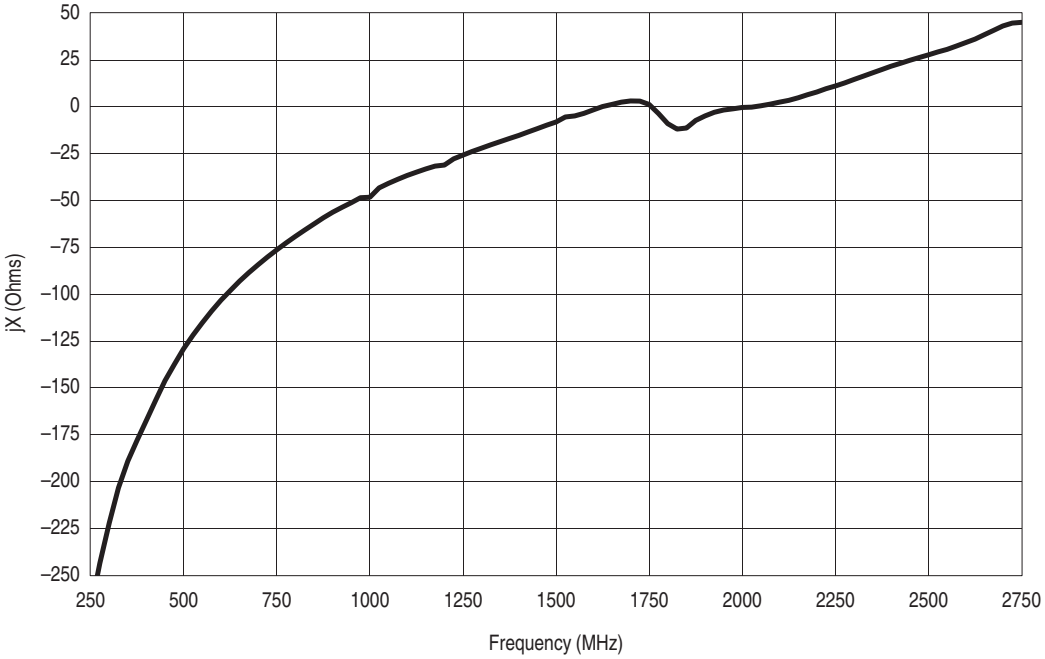
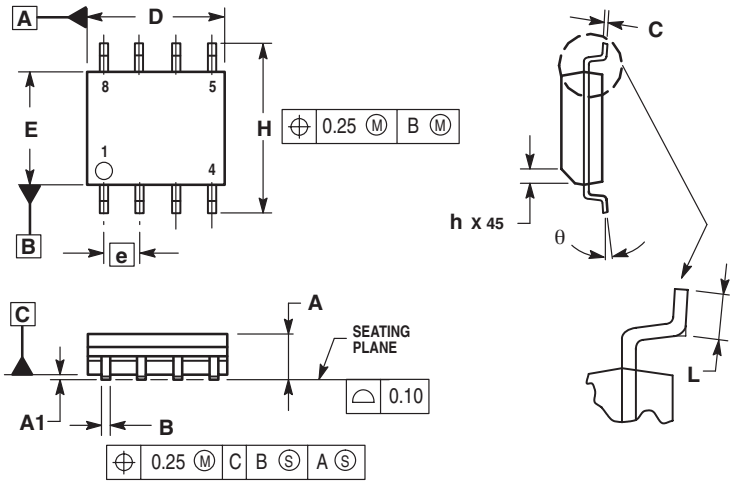


Figure 18. Typical Imaginary Input Impedance versus Input Frequency
(For the F_{in} Input)



OUTLINE DIMENSIONS

SO 8 = -5P
PLASTIC PACKAGE
CASE 751-06
(ML12179-5P)
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°