

ML12079 2.8 GHz Prescaler MECL PLL Components ÷64/128/256 Prescaler

Legacy Device: Motorola MC12079

The ML12079 is a single modulus divide by 64, 128, 256 prescaler for low power frequency division of a 2.8 GHz (typical) high frequency input signal. Divide ratio control inputs SW1 and SW2 select the required divide ratio of \div 64, \div 128, or \div 256.

An external load resistor is required to terminate the output. A 1.2 $k\Omega$ resistor is recommended to achieve a 1.6 V_{pp} output swing, when dividing a 1.1 GHz input signal by the minimum divide ratio of 64, assuming a 12 pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V_{out} specification for various divide ratios at 2.8 GHz input frequency.

- 2.8 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Supply Current 9mA Typical at $V_{CC} = 5.0 \text{ V}$
- Operating Temperature Range of $T_A = -40$ to $85^{\circ}C$

FUNCTIONAL TABLE

SW1	SW2	Divide Ratio
н	н	64
н	L	128
L	н	128
L	L	256

NOTE: SW1 & SW2: $H = V_{CC}$, L = Open.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	VCC	-0.5 to 7.0	Vdc
Operating Temperature Range	TA	-40 to 85	°C
Storage Temperature Range	T _{stg}	-65 to 150	°C
Maximum Output Current, Pin 4	IO	4.0	mA





ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = -40 to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave)		ft	0.25	3.4	2.8	GHz
Supply Current Output (Pin 2)		ICC	-	9.0	11.5	mA
Input Voltage Sensitivity	250–500 MHz 500–2800 MHz	V _{in}	400 100		1000 1000	mVpp
Divide Ratio Control Input High (SW)		V _{IH}	V _{CC}	V _{CC}	VCC	V
Divide Ratio Control Input Low (SW)		VIL	Open	Open	Open	-
Output Voltage Swing $\begin{array}{l} (C_L = 12 \text{ pF}; \text{ R}_L = 1.2 \text{ k}\Omega; \text{ I}_O = 2.7 \text{ mA})^{1} \\ (C_L = 12 \text{ pF}; \text{ R}_L = 2.2 \text{ k}\Omega; \text{ I}_O = 1.5 \text{ mA})^{2} \\ (C_L = 12 \text{ pF}; \text{ R}_L = 3.9 \text{ k}\Omega; \text{ I}_O = 0.85 \text{ mA})^{3} \end{array}$		V _{out}	1.0	1.6	-	V _{pp}

NOTES: 1. Divide ratio of ÷64 at 2.8 GHz. 2. Divide ratio of ÷128 at 2.8 GHz. 3. Divide ratio of ÷256 at 2.8 GHz.

Figure 1. Logic Diagram (ML12079)





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