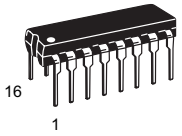
LANSDALE Semiconductor, Inc.

ML12061
Crystal Oscillator

Legacy Device: *Motorola MC12061*

The ML12061 is for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

- Frequency Range = 2.0 to 20 MHz
- Operating Temperature Range = 0 to + 70°C
- Single Supply Operation: +5.0 Vdc or –5.2 V DC
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVpp typ)
  2. Complementary MECL
  3. Single Ended TTL



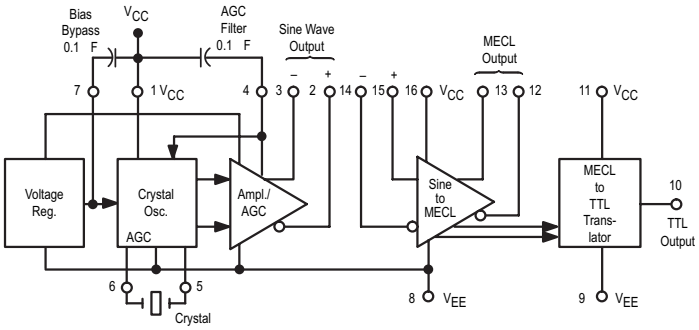
P DIP 16 = EP
PLASTIC PACKAGE
CASE 648

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 16	MC112061P	ML12061EP

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

Figure 1. Block Diagram



Note: 0.1 F power supply pin bypass capacitors not shown.

TYPICAL CIRCUIT CONFIGURATIONS

Note: 0.1 μF power supply pin bypass capacitors not shown.

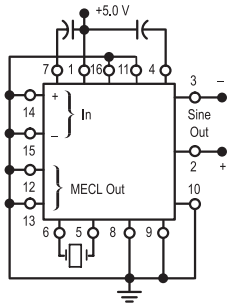


Figure 2. Sine Wave Output

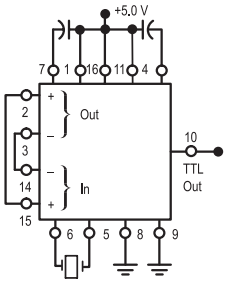


Figure 3. MTTL Output

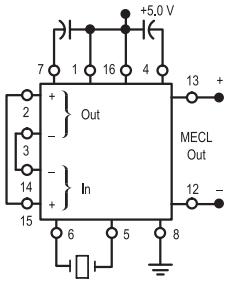


Figure 4. MECL Output
(+5.0 V Supply)

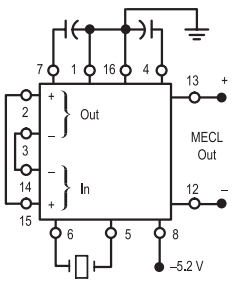


Figure 5. MECL Output
(–5.2 V Supply)

CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	ML12061
Mode of Operation	Fundamental Series Resonance
Frequency Range	2.0 MHz — 20 MHz
Series Resistance, R1	Minimum at Fundamental
Maximum Effective Resistance $R_{E(max)}$	155 ohms

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			0 C		+25 C			+75 C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_{CC}	1	–	–	13	16	19	–	–	mAdc
		1 11 16	– – –	– – –	18 – 13	23 3.0 16	28 4.0 19	– – –	– – –	
Input Current	I_{inH}	14 15	– –	– –	– –	– –	250 250	– –	– –	Adc
	I_{inL}	14 15	– –	– –	– –	– –	1.0 1.0	– –	– –	Adc
Differential Offset Voltage	ΔV	4 to 7 2 to 3	– –	– –	40 –200	– 0	325 +200	– –	– –	mAdc
Output Voltage Level	V_{out}	2 3	– –	– –	– –	3.5 3.5	– –	– –	– –	Vdc
Logic ‘1’ Output Voltage	V_{OH1} (Note 1)	12 13	4.0 4.0	4.16 4.16	4.04 4.04	– –	4.19 4.19	4.1 4.1	4.28 4.28	Vdc
	V_{OH2}	10	2.4	–	2.4	–	–	2.4	–	
Logic ‘0’ Output Voltage	V_{OL1} (Note 1)	12 13	2.98 2.98	3.43 3.43	3.0 3.0	– –	3.44 3.44	3.02 3.02	3.47 3.47	Vdc
	V_{OL2}	10 10	– –	0.5 0.5	– –	– –	0.5 0.5	– –	0.5 0.5	
Logic ‘1’ Threshold Voltage	V_{OHA}	12 13	3.98 3.98	– –	4.02 4.02	– –	– –	4.08 4.08	– –	Vdc
Logic ‘0’ Threshold Voltage	V_{OLA}	12 13	– –	3.45 3.45	– –	– –	3.46 3.46	– –	3.49 3.49	Vdc
Output Short Circuit Current	I_{OS}	10	20	60	20	–	60	20	60	mAdc

NOTE: 1. Devices will meet standard MECL logic levels using V_{EE} = –5.2 Vdc and V_{CC} = 0.

ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE/CURRENT VALUES						
			Volts						
@ Test Temperature			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	
0 C			4.16	3.19	3.86	3.51	4.0	4.75	
+25 C			4.19	3.21	3.90	3.52	4.0	4.75	
+75 C			4.28	3.23	3.96	3.55	4.0	4.75	
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
Characteristic	**Symbol**	**Pin Under Test**	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	**Gnd**
Power Supply Drain Current	I_{CC}	1	–	–	–	–	–	–	8
		1 11 16	– 14 –	– 15 –	– – –	– – –	– – –	– – –	8 8,9 8
Input Current	I_{inH}	14 15	14 15	15 14	– –	– –	– –	– –	8 8
	I_{inL}	14 15	15 14	– –	– –	– –	– –	– –	8,14 8,15
Differential Offset Voltage	ΔV	4 to 7 2 to 3	– –	– –	– –	– –	5,6 4	– –	8 –
Output Voltage Level	V_{out}	2 3	– –	– –	– –	– –	4 4	– –	8 8
Logic ‘1’ Output Voltage	V_{OH1} (Note 1)	12 13	14 15	15 14	– –	– –	– –	– –	8 8
	V_{OH2}	10	15	14	–	–	–	11,16	8,9
Logic ‘0’ Output Voltage	V_{OL1} (Note 1)	12 13	15 14	14 15	– –	– –	– –	– –	8 8
	V_{OL2}	10 10	14 14	15 15	– –	– –	– –	11,16 –	8,9 8,9
Logic ‘1’ Threshold Voltage	V_{OHA}	12 13	– –	– –	14 15	15 14	– –	– –	8 8
Logic ‘0’ Threshold Voltage	V_{OLA}	12 13	– –	– –	15 14	14 15	– –	– –	8 8
Output Short Circuit Current	I_{OS}	10	15	14	–	–	–	11,16	8,9,10

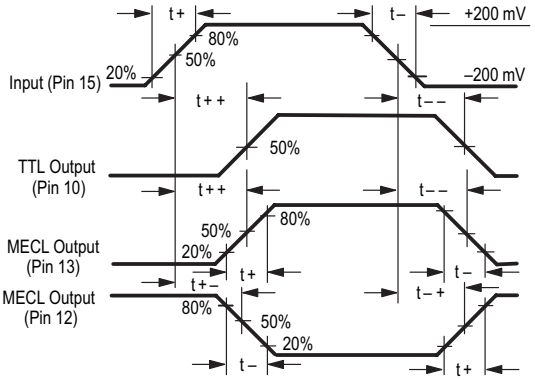
NOTE: 1. Devices will meet standard MECL logic levels using V_{EE} = –5.2 Vdc and V_{CC} = 0.

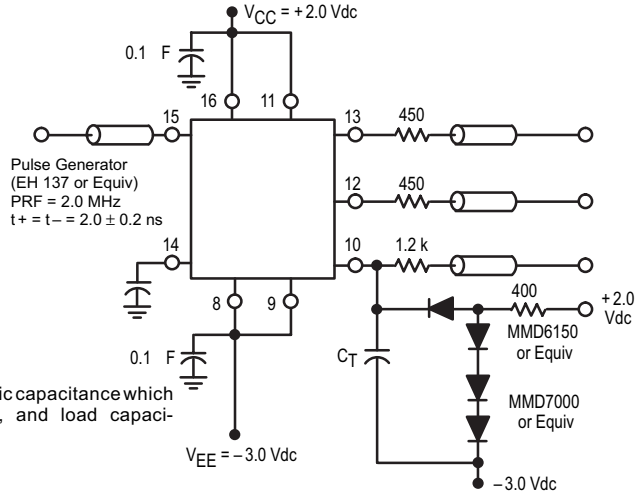
ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE/CURRENT VALUES					
			Volts		mA			
@ Test Temperature			**V_{CC}**	**V_{CCH}**	**I_{OL}**	**I_{OH}**	**I_{IL}**	
0 C			5.0	5.25	16	–0.4	–2.5	
+25 C			5.0	5.25	16	–0.4	–2.5	
+75 C			5.0	5.25	16	–0.4	–2.5	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					
			V_{CC}	**V_{CCH}**	**I_{OL}**	**I_{OH}**	**I_{IL}**	**Gnd**
Power Supply Drain Current	I_{CC}	1	1	–	–	–	–	8
		1 11 16	1 11,16 16	– – –	– – –	– – –	– – –	8 8,9 8
Input Current	I_{inH}	14 15	16 16	– –	– –	– –	– –	8 8
	I_{inL}	14 15	16 16	– –	– –	– –	– –	8,14 8,15
Differential Offset Voltage	ΔV	4 to 7 2 to 3	1 –	– –	– –	– –	– –	8 –
Output Voltage Level	V_{out}	2 3	1 1	– –	– –	– –	– –	8 8
Logic ‘1’ Output Voltage	V_{OH1} (Note 1)	12 13	16 16	– –	– –	– –	12 13	8 8
	V_{OH2}	10	–	–	–	10	–	8,9
Logic ‘0’ Output Voltage	V_{OL1} (Note 1)	12 13	16 16	– –	– –	– –	12 13	8 8
	V_{OL2}	10 10	– –	– 11,16	10 10	– –	– –	8,9 8,9
Logic ‘1’ Threshold Voltage	V_{OHA}	12 13	16 16	– –	– –	– –	12 13	8 8
Logic ‘0’ Threshold Voltage	V_{OLA}	12 13	16 16	– –	– –	– –	12 13	8 8
Output Short Circuit Current	I_{OS}	10	–	–	–	–	–	8,9,10

NOTE: 1. Devices will meet standard MECL logic levels using V_{EE} = –5.2 Vdc and V_{CC} = 0.

Figure 6. AC Characteristics – MECL and TTL Outputs





All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Unused outputs are connected to a 50 Ω ± 1% resistor to ground.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

Characteristic	Symbol	Pin Under Test	Test Limits 0 C Min	0 C Max	+25 C Min	+25 C Typ	+25 C Max	+75 C Min	+75 C Max	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Unit	Pulse In	Pulse Out	+2.0 Vdc	–3.0 Vdc	Gnd
Propagation Delay	t_{15+10+}	10	—	22	—	17	25	—	27	ns	15	10	11,16	8,9	14
	t_{15-10-}	10	—	19	—	12	18	—	18			10			
	t_{15+12-}	12	—	5.2	—	4.3	5.5	—	5.8			12			
	t_{15-12+}	12	—	5.0	—	3.7	5.2	—	5.2			12			
	t_{15+13+}	13	—	4.8	—	4.0	5.0	—	5.2			13			
	t_{15-13-}	13	—	5.0	—	4.0	5.0	—	5.1			13			
Rise Time	t_{12+}	12	—	4.0	—	3.0	4.0	—	4.4	ns	15	12	11,16	8,9	14
	t_{13+}	13	—	4.0	—	3.0	4.0	—	4.4	ns	15	13	11,16	8,9	14
Fall Time	t_{12-}	12	—	4.0	—	3.0	4.0	—	4.0	ns	15	12	11,16	8,9	14
	t_{13-}	13	—	4.0	—	3.0	4.0	—	4.0	ns	15	13	11,16	8,9	14

Characteristic	Pin Under Test	+25 C Min	+25 C Typ	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW +2.0 Vdc	–3.0 Vdc
Sine Wave Amplitude	2	650	750	mVp-p	1	8,9
	3	650	750			

Figure 7. AC Test Circuit – Sine Wave Output

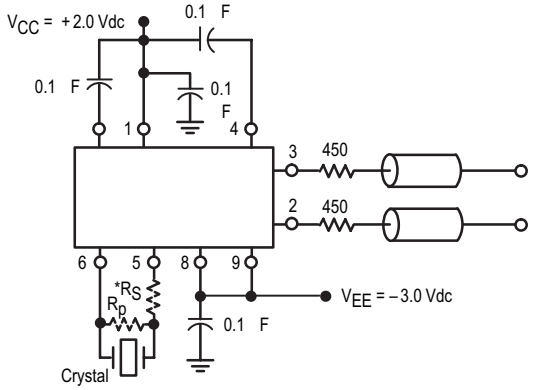
All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 Ω ± 1% resistor to ground.

450 Ω resistor and the scope termination impedance constitute a 10:1 attenuator probe.

Crystal — Reeves Hoffman Series Mode,
Series Resistance Minimum at Fundamental
f = 10 MHz
R_E = 5 Ω

*R_S = 15 kΩ is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance ≤ 155 Ω

R_p: will improve start up problems value: 200–500 Ω



The ML12061 consists of three basic sections: an oscillator with AGC and two translators. Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or TTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal — an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The ML12061 is designed to operate from a single supply — either +5.0 Vdc or –5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the TTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 42 mA to 23 mA for the ML12061.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup. However, the variation should be within approximately ±0.001% from unit to unit. Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small — about –0.08ppm/°C for ML12061 operating at 8.0 MHz.

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mV_{p-p} (no load) to 500 mV_{p-p} (120 ohm AC load). Approximately 500 mV_{p-p} can be provided across 50 ohms by slightly increasing the DC current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15pF) to the 50 ohm load of Figure 9. The DC voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates and the TTL output (pin10) will drive up to ten gates.

Noise Characteristics

Noise level evaluation of the sine wave outputs operation at or 9.0 MHz, indicates the following characteristics:

1. Noise floor (200 kHz from oscillator center frequency) is approximately –122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
2. Close-in noise (100 Hz from oscillator center frequency) is approximately –88 dB when referenced to a 1.0 Hz bandwidth.

Figure 8. Frequency Variation Due to Temperature

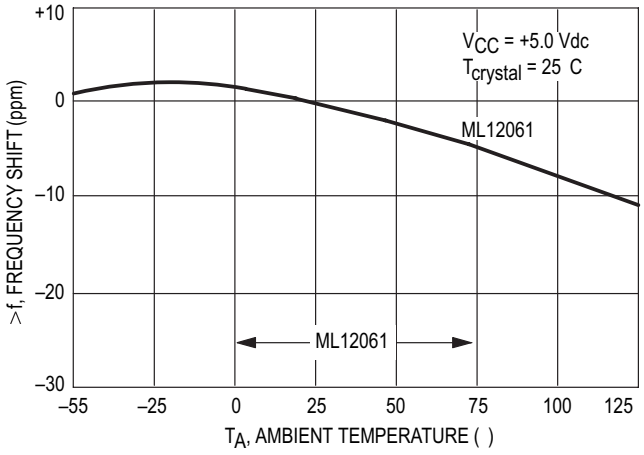
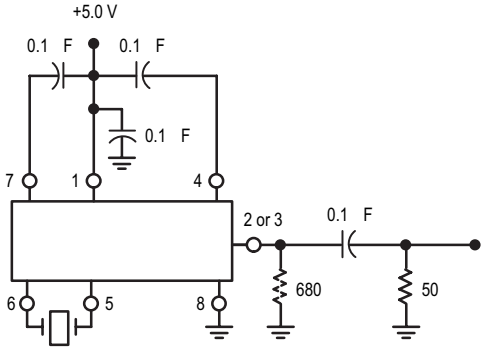


Figure 9. Driving Low Impedance Loads



* See text under signal characteristics.

Figure 10. MECL Translator Load Capability

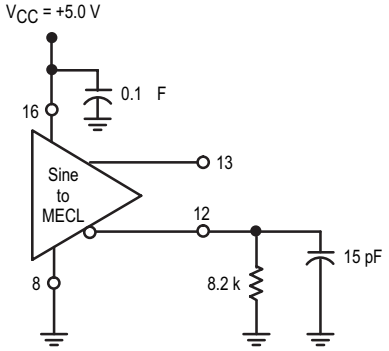


Figure 11. TTL Translator Load Capability

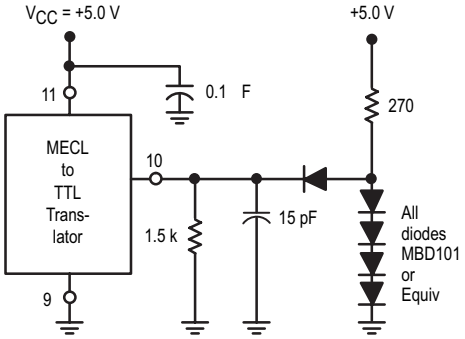
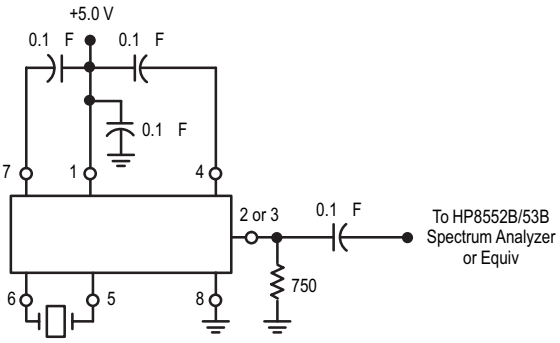


Figure 12. Noise Measurement Test Circuit

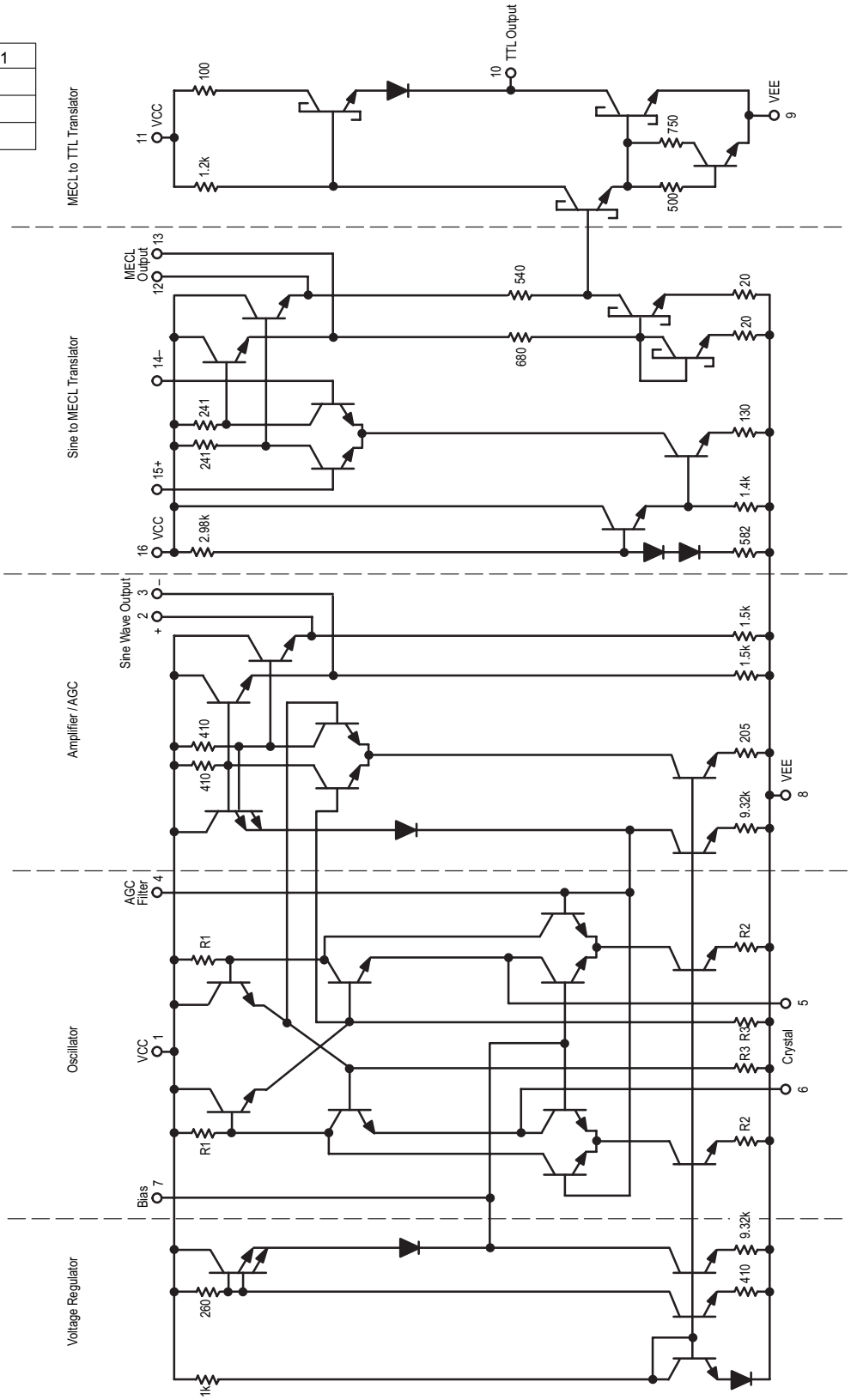


ANALYZER SETTING

Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close-In Noise	20 kHz/div	10 Hz	10 Hz

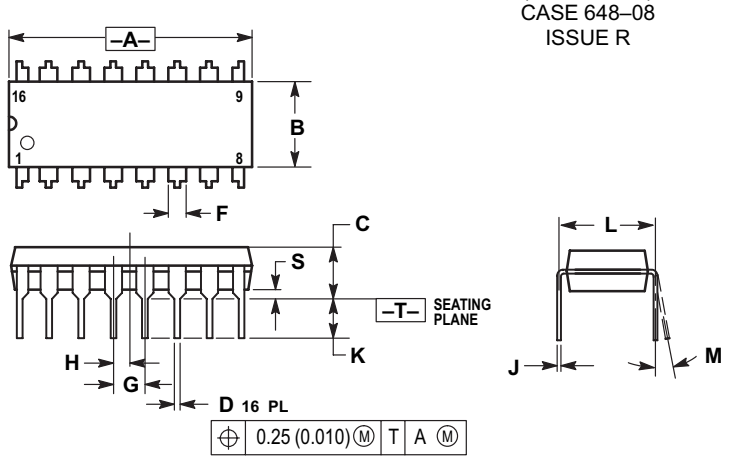
Figure 13. Circuit Schematic

RESISTOR	ML12061
R1 (2 Places)	200 Ω
R2 (2 Places)	400 Ω
R3 (2 Places)	2 kΩ



OUTLINE DIMENSIONS

P DIP 16 = EP
PLASTIC PACKAGE
(ML12061EP)
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01