

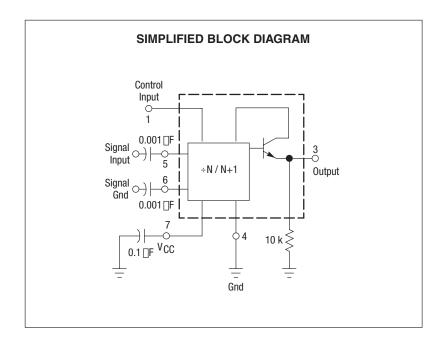
# ML12019 **Dual Modulus Prescaler**

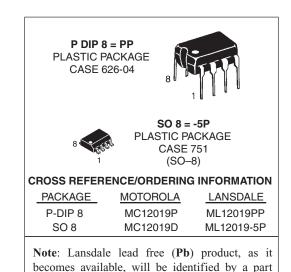
### MECL PLL COMPONENTS ÷20/21 DUAL MODULUS SEMICONDUCTOR TECHNICAL DATA

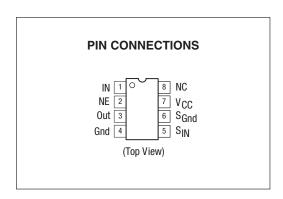
Legacy Device: Motorola MC12019

The ML12019 is a divide by 20 and 21 dual modulus prescaler. It will devide by 20 when the modulus control input is HIGH and divide by 21 when the modulus control input is LOW.

- 225 MHz Toggle Frequency
- Low-Power 7.5 mA Maximum at 5.5 V
- Control Input is Compatible with Standard Motorola or Lansdale CMOS Synthesizers
- Emitter Follower Output
- Operating Temperature Range  $T_A = -40$  to  $85^{\circ}C$







number prefix change from ML to MLE.

#### **MAXIMUM RATINGS**

Rating	Symbol	bol Value	
Power Supply Voltage, Pin 7	VCC	8.0	Vdc
Operating Temperature Range	T <sub>A</sub>	-40 to +85	□C
Storage Temperature Range	T <sub>stg</sub>	-65 to +175	□C

## **ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$ ; $T_A = -40 \text{ to } 85 \text{ C}$ ), unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave Input)	f <sub>max</sub> f <sub>min</sub>	225 -	_ _	- 20	MHz
Supply Current	ICC	_	_	7.5	mA
Control Input HIGH ( ☐20)	VIH	2.0	_	-	V
Control Input LOW ( 21)	V <sub>IL</sub>	-	-	0.8	V
Output Swing Voltage (10 kΩ to ground)	V <sub>out</sub>	600	_	1200	mVpp
Input Voltage Sensitivity 20 MHz to 225 MHz	V <sub>in</sub>	200	_	800	mVpp
PLL Response Time (Notes 1 and 2)	<sup>t</sup> PLL	_	_	t <sub>out</sub> -70	ns

NOTES: 1. tp\_LL = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.

2. tout = period of output waveform.

Figure 1. Generic block diagram showing prescaler connection to PLL device

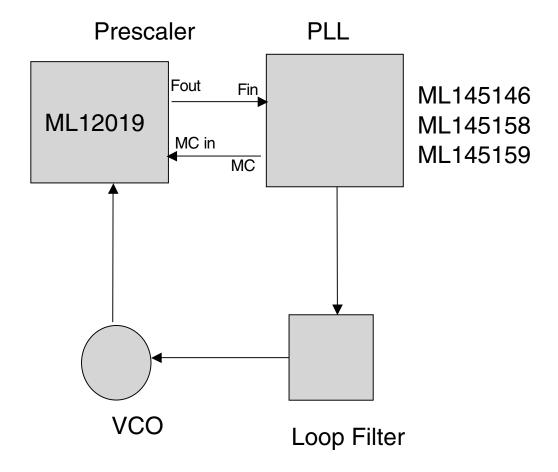
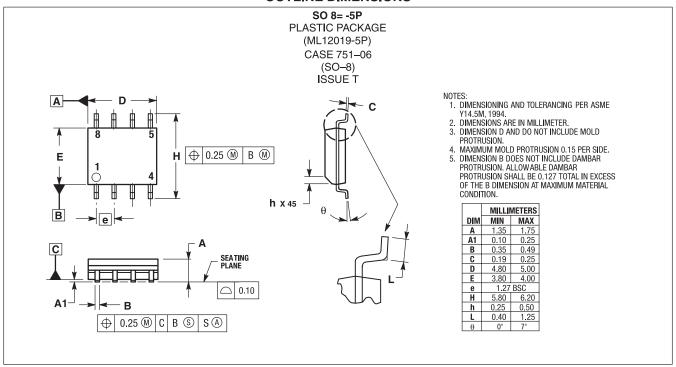
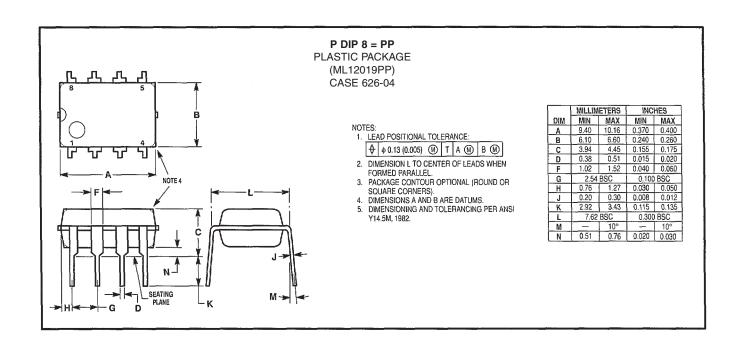


Figure 1 shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 decribes using a two-modulus prescaler technique.By using prescaler higher frequencies can be achieve than by a single CMOS PLL device.

#### **OUTLINE DIMENSIONS**





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